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| --- |
| Text  Description automatically generated  **Submitted by:**  **Name: Hasan Tanveer Mahmood**  **Matric no: 1725413**  **COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE**  **Course: CSC-3402, Sec: 02**  **Lecturer: Dr. HAFIZAH BINTI MANSOR** A picture containing text  Description automatically generated **Lab Exercise - 2** |

**DATE: 21-APR-2021**

**Single Cycle Processor:**

**Diagram, schematic

Description automatically generatedDiagram, schematic

Description automatically generatedFigure 1: xor $s1,$s2,$t2**

**Figure 2: lw $s1, 8($s2)**

Diagram, schematic

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**Figure 3: sw $s1, 8($s2)**

**Diagram, schematic

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**Figure 4: beq $s1,$s2,LABEL**

Diagram, schematic

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**Figure 5: xori $s1,$s2,20**

**References:**

* **For Control Signal Value I took references from:**

Calendar

Description automatically generated with low confidence